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Proton-Induced Single Event Upset Characterization of a 1 Giga-Sample per Second Analog to Digital Converter

R.A. Reed[1], P.W. Marshall[2], M.A. Carts[3], G.L. Henegar[1], R.B. Katz[1]

[1]NASA/GSFC Greenbelt, MD
[2]Consultant
[3]NRL Washington DC

ABSTRACT

Some high-speed space-borne data acquisition and dissemination systems require conversion of an analog data signal into a digital signal for on-board digital processing. The NASA Geoscience Laser Altimeter System (GLAS) is one such instrument. It uses the Signal Processing Technologies SPT7760 to convert an analog signal from the laser altimeter. The analog data is converted by the SPT7760 at 1 Giga-sample per second (Gsps). These types of data handling applications can typically withstand a relatively high bit error ratio (BER). In this paper, we describe the a novel approach for proton-induced single event upset characterization of the SPT7760. Data is given for operating sample rates from 125 Msps to 1 Gsps.

I. INTRODUCTION

Analog to digital converters (ADCs) are used in most space systems in some form or another. For most applications a low speed device, <20 Msps, is more than sufficient. As designs become more aggressive towards faster data acquisition rates, high speed ADC are required. In this paper we will describe one such application used by the design team of the NASA spacecraft called GLAS. The data acquisition rate requirement drove designers to use an ADC that operates at a 1 Gsps.

Several papers that describe single event upset (SEU) characterization methods for ADCs have been published [1 and the references therein]. We relied on these publications to guide us during our test setup phase. However, specific issues with using the SPT7760 converting at 1 Gsps required us to develop a novel testing approach. We will describe the novel approach for collecting experimental SEU information on the ADC. These data included characterization of the duration of the upset or multiple word upsets.

The testing was done at various converter sample rates. General it is believed that for some, if not most microelectronics, there is a SEU cross section dependence on data rate [1,2]. In [2] we describe the data rate dependence for some devices is linear, while for other devices it is not. Reference [1] discusses the data rate dependence for ADCs. The conclusions presented there were that for most flash ADC one would expect a linear dependence, but in certain cases there was inconclusive evidence that the effect of sample frequency on the cross-section was second order. We present SEU data on the SPT7760 from 0.125 Gsps to 1 Gsps for three different input levels.

II. DEVICE DESCRIPTION

The SPT7760 is a fully parallel (flash) analog to digital converter (ADC) with an input range of 0 to –2 V, providing 8 bits of resolution (256 values) with an additional over-range bit. The analog input has a bandwidth of over 900 MHz and a capacitance of < 15 pF. Metastable errors are 1 Least Significant Bit (LSB) according to the datasheet but are < ¼ LSB according to conversations with the manufacturer. The output byte stream is at differential ECL levels, and analog input levels are represented according to a "gray code" to reduce digital signal-induced EMI. The byte stream is demultiplexed into two identical ports (labeled portA and portB) each with 9 bits (8 + overflow) plus clock at a maximum output of 500 Msps per port, for an aggregate throughput of 1 Gsps. The DUT operates from a single –5.2 Volt DC supply, nominally consuming 5.5 W. The package is an 80 pin MQUAD, and the device is available in a MIL-STD 883 screened version. The manufacturer indicates that both a heat sink and a fan are required for operation. Additional information on both the ADC and on the evaluation board can be found at the manufacturer's website (see http://www.spt.com/ datasheets/products/7760.pdf).

III. GLAS'S USE OF THE SPT7760

The primary science objective of the GLAS instrument is to obtain day & night, long-term spaceborne ice sheet topography measurements with sufficient spatial and temporal resolution to detect regional elevation changes. The GLAS instrument will orbit the Earth at a altitude of 600 kilometers. The altimetry subsystem of the instrument uses a high-powered laser and sophisticated optical receiver to detect the outgoing laser pulse and the return signal reflected from the Earth. The SPT7760 digitizes these signals at the 1 Gsps rate that achieves the required 10 cm resolution.

The SPT 7760 is part of the Altimeter Digitizer subsystem within the GLAS Instrument electronics, Figure 1. In addition to the high-speed A/D converter, this subsystem also contains a Digital Signal Processor and custom Finite Impulse Response (FIR) filter gate array that processes the digitized waveforms to determine the locations of the outgoing and return signals within the data. This information is passed to the Instrument Computer where the data is packaged for transmission to the ground station at the next ground contact.

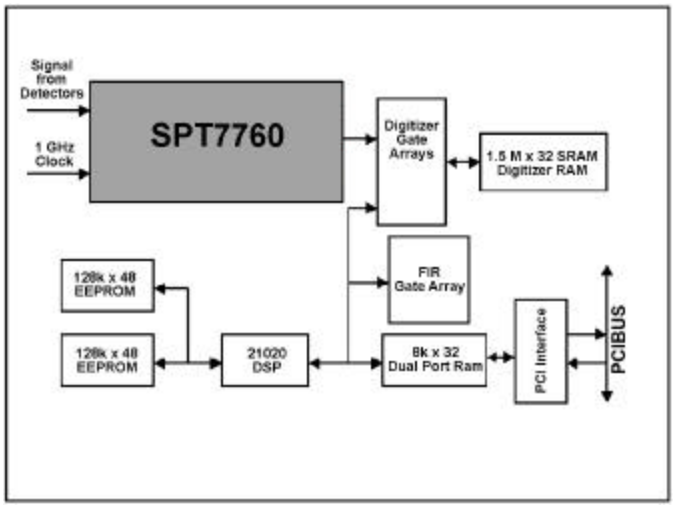

Figure 1: Use of SPT7760 in GLAS Instrument.

IV. EXPERIMENTAL SETUP

The high sample rates associated with 1 Gsps operation preclude raw storage of the data and post-processing to evaluate SEE performance. This, plus additional complexities encountered when operating with dynamic input conditions, indicated the need for a pseudo-static test approach. The approach we adopted involved setting the analog input to a given, static, level, flowing the samples through a FIFO, and comparing consecutive samples for a change in value. Upon detection of a change, the FIFO is frozen, storing the evidence of an SEU for the controller to capture. The full paper will describe the customized ECL-based test board and software designed to implement this and capture full error histories including pre-trigger conditions and error progression over multiple clock cycles.

A. Test Hardware Description

Proton testing of the SPT 7760 ADC utilized the manufacture-supplied evaluation board (SPT EB7760) which provided two 500 Msps DUT outputs corresponding to ports A and B as previously indicated. The high data rate from the DUT during operation precludes storage of raw data for post-processing, so a set of custom high speed boards were designed to interface to the 7760 evaluation board and capture only the information characteristic of single event induced errors. These boards (one for each of the two DUT output ports) capture the error details and provide the error history to a low speed interface for recording and analysis. A diagram of the test approach is provided a Figure 2. The figure depicts a static input signal to the DUT followed by buffered outputs from the DUT evaluation board and high speed ribbon cable connections to the custom processor boards. The high speed processor boards capture the SEE data make it available for storage via digital interface cards with control through a VXI chassis. All components remote to the VXI control are accessed through GPIB connections and controlled via LABVIEW®-based software.

Since on-the-fly comparison of converted, changing analog values from both the DUT and an input reference is impracticable because of non-reproducible inter-bit uncertainty, the test depicted in Figure 3 was implemented using static input conditions to the DUT. This compromise was made with the recognition that some categories of errors, from SEEs in clock distribution circuitry, might not be captured. Consequently, the test instrumentation provided DC bias levels to the DUT with the ability to change bias conditions

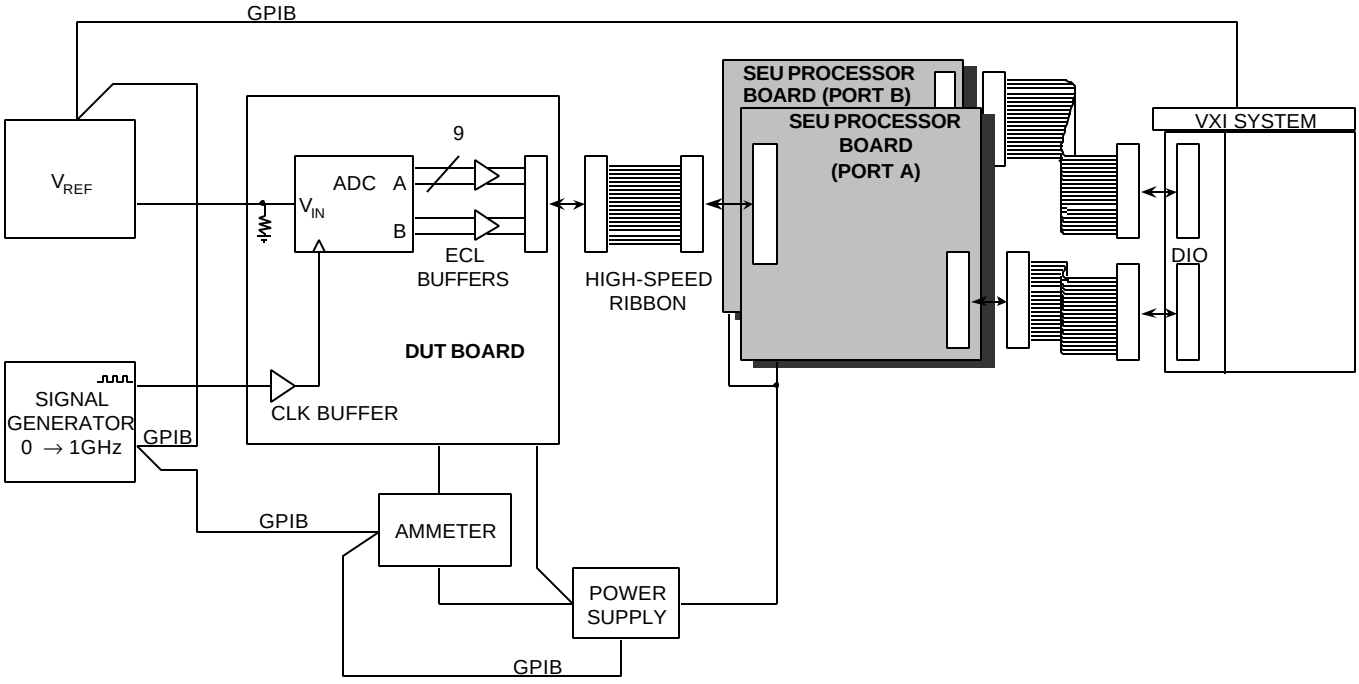

Figure 2. Test Set Configuration.

prior to data acquisition. It was a key requirement of the test hardware to be able to identify not only that a change in ADC output from an SEE had occurred, but also the number clock cycles needed for an error condition to be corrected.

With two high speed boards monitoring the two output channels of the DUT, each board captured one of two 9-bit wide byte streams at a rate of up to 500 Msps. Figure 3 shows the operation of the two high speed SEE data capture boards, and each board was dedicated to one of the two DUT output ports. These were 6-layer controlled impedance boards fabricated using FR-4 material. The two primary functions of each board were to first determine that an SEE event had occurred and next capture the SEE details for low speed interface interrogation and data logging. A SEE event was identified by a change in the gray code output while a static input was maintained. This was determined by the state machine in the top right portion of Figure 3. The x-or logic function provides a trigger indicating that the most recent DUT output differs from the output captured during the previous clock cycle.

Once a SEE was identified by a change in the DUT output, the correct output, along with the erroneous condition was saved in FIFO memory. The FIFO operated using the high speed board clock in the absence of an SEE, but the trigger from the x-or function indicating an event disabled the FIFO clock and "froze" the event in memory after a selectable delay (i.e., number of clock cycles). Either of the two high speed boards could determining the occurrence of an SEE and halt its own FIFO clock as well as the other board's FIFO clock. With the entire error progression now captured in FIFO on the two boards, a low speed clock provided via the VXI interface allowed the FIFOs to be downloaded into hard drive memory via the digital interface to the controlling VXI chassis. The state machine captured all changes during a given test, and the 9 x 9 FIFO captured the duration of the event for up to 9 clock cycles on a given channel (18 samples across both channels).

The hardware described in the two figures was operated at several fixed clock frequencies from 10 MHz to 1 GHz and with several fixed static input conditions to comprise a matrix of test conditions.

B. Software Description

The application software was written in National Instruments' LABVIEW®- environment. The operator interface consists of controls (inputs) and indicators (outputs). Simple controls for the custom boards include mask bits, reset, slow clock, clock select, and error injector. Meta-controls were added in order to facilitate easier operation of various tasks, such as processing one SEU (switching the clock, reading the FIFO, resetting the circuitry and switching the clock back). Indicators include the data byte and the status of the STOP signal. Controls and indicators for operating the analog input voltage source, as well as indicators for displaying SEU data and controls for the storage, display, and annotation of the data, were incorporated. The graphical user interface to the hardware is shown as Figure 4.

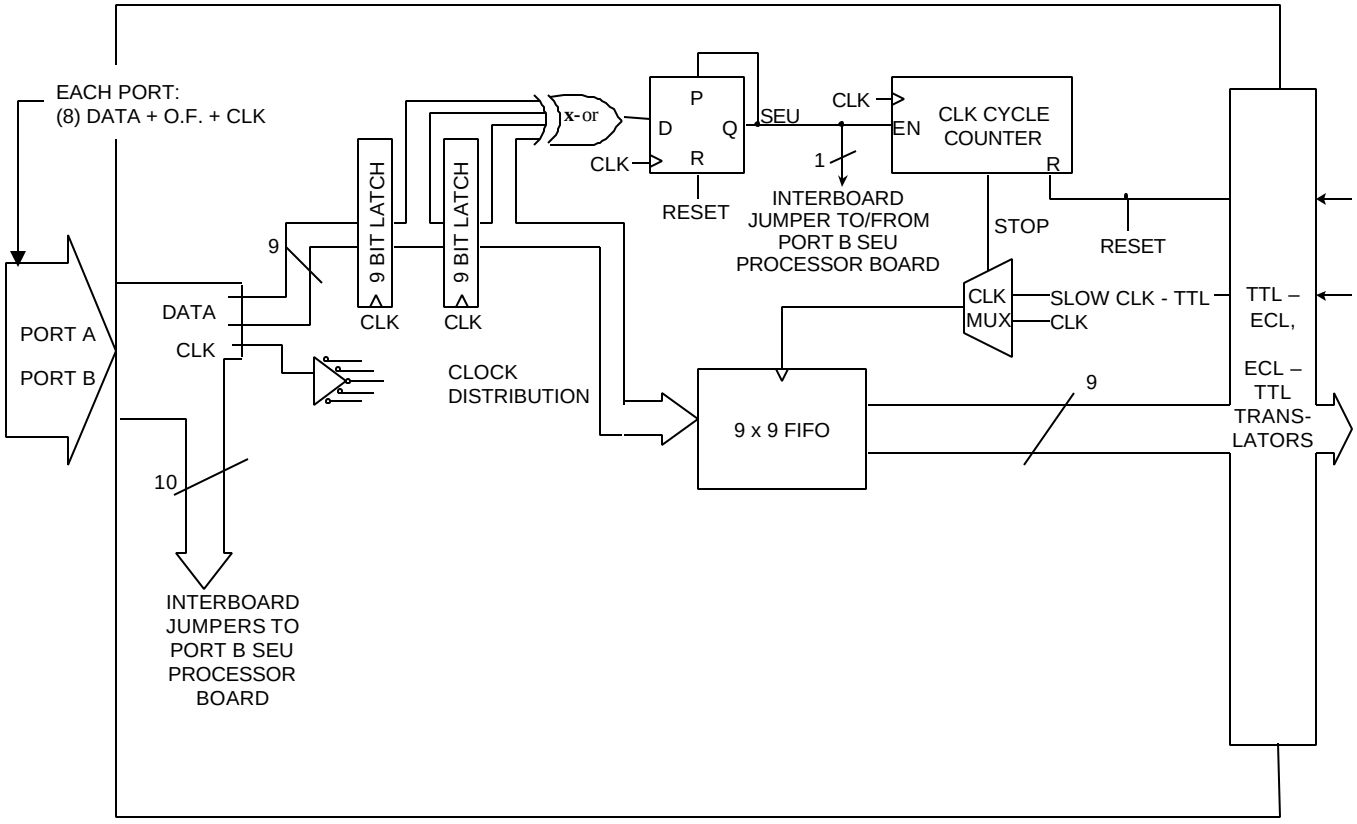

Figure 3: PortA SEU Processor Board.

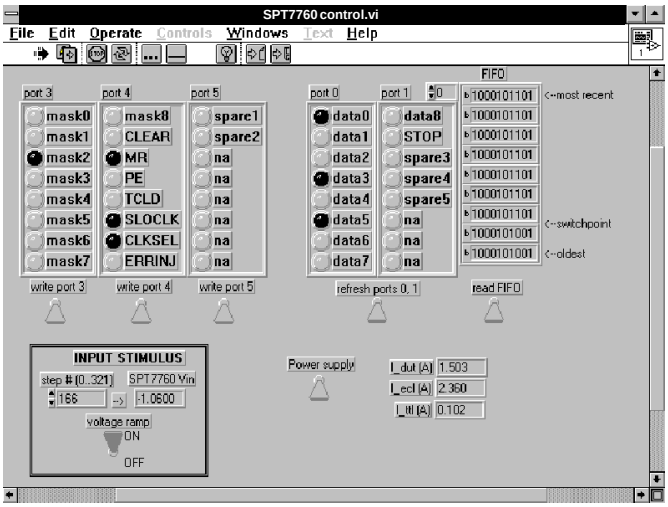

Figure 4: Computer display for STP7760 control.vi.

Data management is conducted as follows: The data from the two boards are interleaved (multiplexed--it was demultiplexed in the ADC) and stored in a data file, along with operator annotations. The data (18 bytes) is stored in a matrix, and is displayed in binary and decimal formats of the gray-coded and the de-gray-coded representations, for both the individual ports and the interleaved data. The matrix can be emptied, and the existing data can be binned and displayed in histograms in various ways. Post-processing software reads the data files, de-interleaves the data (the identity of port A and port B is lost, of course) and provides the same analysis, in addition to displaying the annotations.

V. RESULTS AND DISCUSSION

The Crocker Nuclear Laboratory's proton facility at the University of California at Daves was used to performed at 63 MeV proton irradiations. Figure 5 gives the measured cross section as a function of sample rate for various input levels for device under test #1 (DUT #1). Test setup hardware limited data collection to less than 1 Gsps. The data is clearly nonlinear for all cases. However, these data do show a little structure in that for some cases tested the cross section dips slightly near 500 Msps. For the given input levels, the variation with sample rate is less than a factor of three. The non-linear response over sample rate is somewhat surprising when comparing this data to other ADCs [1] and ECL [2] devices. Also, notice the SEU cross sections are relatively low. This is another surprising result when comparing this to previous tested ECL devices [2,3].

The low values of the measured cross section will result in a relatively low proton-induced SEU rate. In [1] it was recommend that one use a linear correction for SEU rates computed for ADCs. However, we do not recommend using a linear correction for devices that do not show a linear response over sample rate. To compute rates for devices that exhibit a non-linear response we recommend that SEU testing be carried out over all operating sample rates for the application. Then use the standard methods for computing rates such as Bendel approach for proton-induced events and the integral right rectangular parallelepiped (IRPP) model for the heavy-ion rate predictions for each data rate.

Testing was done to look for proton-induced ionizing dose effects on the functionality of the SPT7760. Two devices where irradiated, one to 160 krad(Si) and the other to 580 krad(Si). Both devices remained functional with no measurable increase in DUT current. Figure 6 gives the measured cross-section over total ionizing dose for the two DUTS. Data on DUT #1 is represented by squares. These data are at a fixed input voltage of –1V and for various sample rates. Data on DUT #2 is represented by diamonds while operating at a fixed input voltage of –1V and a fixed sample rate of 1 Gsps. There was < 20% change in the measured cross section for DUT #2 over total dose, except at the highest dose level.

An SEU is essentially a jump in the output code of the ADC. Figure 7 is a histogram of the number of times a radiation event caused a wrong code when the DUT was operated at 1000 Msps. Figure 8 is the same for the DUT operating at 125 Msps. The input was the same for both cases (-1V). Comparing these data show that there is no observable difference over frequency for code jumps. Recoils from spallation reactions have LETs less than 15 MeV – cm^2 / mg. Data taken by other experimenters on other ADCs show that

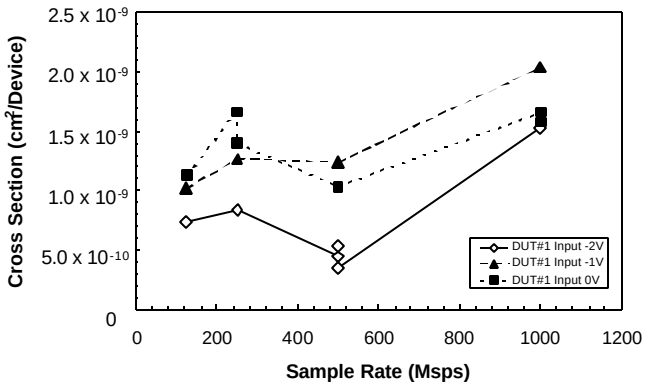

Figure 5: Cross-section for upset at various data rates for three input levels.

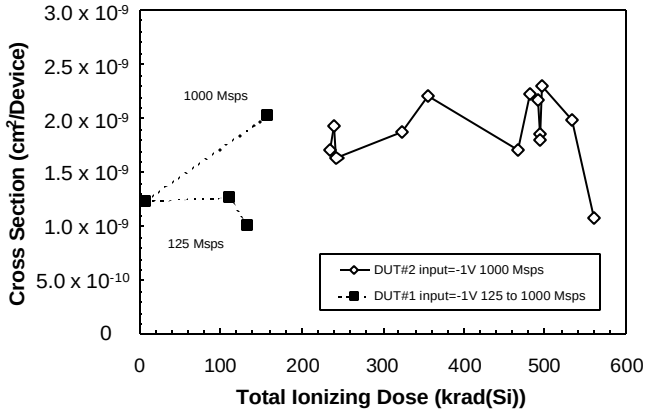

Figure 6: Measured cross section over total dose.

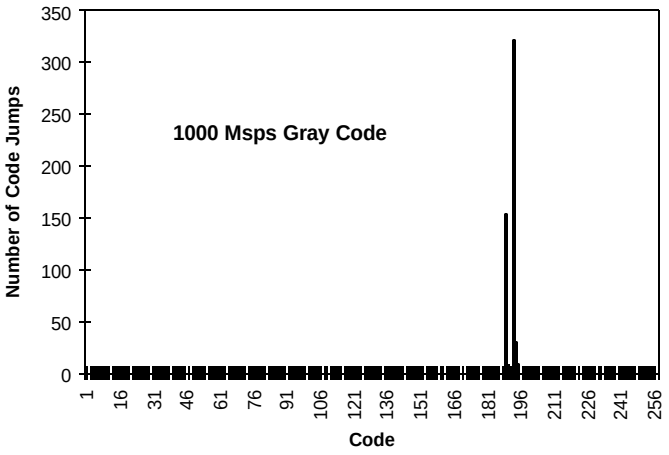

Figure 7: Code jumps at 1 Gsps expected code 191.

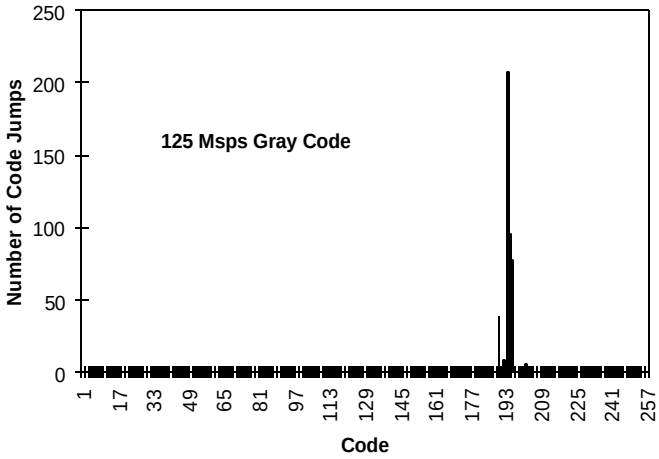

Figure 8: Code jumps at 0.125 Gsps expected code 191.

these histograms change as LET is increased [1]. Low LET particles typically induce small jumps in code, while higher LET particles will produce large and small jumps in the output code. Figures 7 and 8 agree with these analyses for low LET particles. These data are consistent with event occurring on the analog portion of the ADC [1]. One would expect that heavy ion testing at higher LETs could result in a histogram of events that is much different as the digital portion of the ADC becomes sensitive.

During testing we observed multiple word errors. The 8 bit output of the device would be a value different than the expected value for several clock cycles. At 125 Msps this type of event was rare, only occurring once during and exposure of $4x10^{11}$ p/cm^2. In contrast, during an exposure of $3x10^{11}$ p/cm^2 with the device operating at identical conditions except the sample rate, which was 1 Gsps, the data shows SEUs that last up to 7 clock cycles. And at least 55 of the 513 events were greater than one clock cycle.

VI. CONCLUSIONS

In this paper we provide a description of a novel characterization method for 1 Gsps ADCs. The new data collected on a 1 Gsps ADC provides evidence of a non-linear response over sample rate, a surprising result. The data shows that this device has a relative low cross section for proton-induced SEUs and remains functional at a proton dose of 580 krad(Si). The data also shows a frequency dependence on the duration of an SEU. At higher frequencies events tended to extended beyond one clock cycle.

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